In the claims:

All claims in the application are indicated below.

Claims 1-17 (Canceled)

18. (Original) A method of transferring a charge from a charge accumulation layer to a transistor of a solid picture element so as to substantially eliminate residual images, comprising the steps:

locating a charge accumulation region of a first conductive type within a semiconductor substrate having a first surface such that no portion of the charge accumulation region contacts the first surface of the semiconductor substrate;

locating a depletion prevention region within the semiconductor substrate between the charge accumulation region and the first surface;

locating a transfer gate on the first surface of the semiconductor substrate such that the transfer gate overlaps a portion of the charge accumulation region; and

locating a transistor within the semiconductor substrate, the transistor being in communication with the transfer gate for receiving a charge from the charge accumulation region and amplifying the charge.

19. (Original) The method of claim 18 further comprising the step of locating the charge accumulation region so as to orient a first margin of the charge accumulation region toward the transistor and locating the depletion prevention region so that no portion of the depletion prevention region is closer to the transistor than the first margin of the charge accumulation region.

20. (Original) The method of claim 18 further comprising the step locating a first margin of the charge accumulation region 0.0 to 0.2 μm closer to the transistor than any portion of the depletion prevention region.

21. (Original) The method of claim 18 wherein the transistor is a field effect transistor.

22. (Original) The method of claim 18 wherein the transistor is a bipolar transistor.

23. (Original) The method of claim 18 wherein the transistor is a metal-oxide semiconductor transistor.

24. (Original) The method of claim 18 wherein the transfer gate is a metal-oxide semiconductor gate.

40. (Previously added) A method of manufacturing a solid picture element having a semiconductor substrate of a first conductive type with a first surface, a transistor located within the semiconductor substrate for amplifying charges, a charge accumulation region of a second conductive type located within the semiconductor substrate, the charge accumulation region having a margin located a first distance from the transistor, a depletion prevention region of the first conductive type located between the charge accumulation region and the first surface of the semiconductor substrate, the depletion prevention region having a margin located a second distance from the transistor, and a transfer gate located on the first surface of the semiconductor substrate between the depletion prevention region and the transistor overlapping a portion of the depletion prevention region margin and the charge accumulation region margin, the charge accumulation region margin being closer to the transistor than the depletion prevention margin, the transfer gate controlling transfer of charges from the charge accumulation region to the transistor, the substrate and the depletion prevention region have different impurity concentrations, the method comprising the steps:

implanting ions of the first conductive type at a first angle to the first surface of the semiconductor substrate using the transfer gate as a mask and forming the charge accumulation region such that it is within the semiconductor substrate and doesn't contact the first surface of the semiconductor substrate; and

implanting ions of the second conductive type at a second angle to the first surface of the semiconductor substrate using the transfer gate as a mask and forming the depletion prevention region such that it is between the charge accumulation region and the first surface of the semiconductor substrate;

wherein the first angle is not greater than the second angle, thereby causing the first distance of the charge accumulation region margin to the transistor to be no greater than the second distance of depletion prevention region margin to the transistor.

41. (Previously added) The method of claim 40 wherein the first angle is between 30 degrees and 80 degrees and the second angle is substantially 90 degrees.

42. (Previously added) The method of claim 40 wherein the first angle is between 40 degrees and 60 degrees and the second angle is substantially 90 degrees.

43. (Previously added) The method of claim 40 wherein the first angle is between 30 degrees and 80 degrees and the second angle is between 80 degrees and 90 degrees.

44. (Previously added) The method of claim 40 wherein the first angle and the second angle are substantially equal and the charge accumulation region margin and the depletion prevention region margin are substantially the same distance from the transistor.

45. (Previously added) The method of claim 40 wherein the second distance of the depletion region margin to the transistor is between 0.0 μm and 0.2 μm greater than the first distance of the charge accumulation region margin to the transistor.

46. (Previously added) The method of claim 40 wherein the depth of the charge accumulation region from the first surface is between 0.6 μm and 0.8 μm and the maximum impurity concentrations of the charge accumulation region is

between 1 x 10^{17} and 2 x 10^{17} per cm^3, and the first angle is between 66 degrees and 75 degrees and the second angle is between 80 degrees and 90 degrees.

47. (Withdrawn) A method of manufacturing a solid picture element having a semiconductor substrate of a first conductive type with a first surface, a transistor located within the semiconductor substrate for amplifying charges, a charge accumulation region of a second conductive type located within the semiconductor substrate, the charge accumulation region having a margin located a first distance from the transistor, a depletion prevention region of the first conductive type located between the charge accumulation region and the first surface of the semiconductor substrate, the depletion prevention region having a margin located a second distance from the transistor, and a transfer gate located on the first surface of the semiconductor substrate between the depletion prevention region and the transistor overlapping a portion of the depletion prevention region margin and the charge accumulation region margin, the charge accumulation region margin being closer to the transistor than the depletion prevention margin, the transfer gate controlling transfer of charges from the charge accumulation region to the transistor, the substrate and the depletion prevention region have different impurity concentrations, the method comprising the steps:

implanting ions of the first conductive type into the semiconductor substrate using the transfer gate as a mask and forming the charge accumulation region such that it is within the semiconductor substrate and doesn't contact the first surface of the semiconductor substrate;

locating an oxide film on the transfer gate thereby increasing the footprint of the transfer gate on the first surface of the semiconductor substrate; and

implanting ions of the second conductive type into the semiconductor substrate using the transfer gate with oxide film as a mask and forming the depletion prevention region such that it is between the charge accumulation region and the first surface of the semiconductor substrate, and the first distance

of the charge accumulation region margin to the transistor is no greater than the second distance of depletion prevention region margin to the transistor.

48. (Withdrawn) The method of claim 47 further comprising the step of selecting a thickness of the oxide film so that the second distance is not more than 0.2 μm greater than the first distance.

49. (Withdrawn) The method of claim 47 further comprising the step of selecting a thickness of the oxide film so that the first distance is approximately 0.1 μm less than the second distance

50. (Withdrawn) A method of manufacturing a solid picture element having a semiconductor substrate of a first conductive type with a first surface, a transistor located within the semiconductor substrate for amplifying charges, a charge accumulation region of a second conductive type located within the semiconductor substrate, the charge accumulation region having a margin located a first distance from the transistor, a depletion prevention region of the first conductive type located between the charge accumulation region and the first surface of the semiconductor substrate, the depletion prevention region having a margin located a second distance from the transistor, and a transfer gate located on the first surface of the semiconductor substrate between the depletion prevention region and the transistor overlapping a portion of the depletion prevention region margin and the charge accumulation region margin, the charge accumulation region margin being closer to the transistor than the depletion prevention margin, the transfer gate controlling transfer of charges from the charge accumulation region to the transistor, the substrate and the depletion prevention region have different impurity concentrations, the method comprising the steps:

implanting ions of the first conductive type into the semiconductor substrate using the transfer gate as a mask and forming the charge accumulation region such that it is within the semiconductor substrate and does not contact the first surface of the semiconductor substrate;

locating and etching an insulating film on an end wall of the transfer gate; and

implanting ions of the second conductive type into the semiconductor substrate using the insulating film as a mask and forming the depletion prevention region such that it is between the charge accumulation region and the first surface of the semiconductor substrate, and the first distance of the charge accumulation region margin to the transistor being no greater than the second distance of depletion prevention region margin to the transistor.

51. (Withdrawn) The method of claim 50 further comprising the step of locating and etching the insulating film so that the first distance is not less than 0.1 μm of the second distance.

52. (Withdrawn) The method of claim 50 further comprising the step of implanting the ions of the second conductive type at an angle to the first surface.

53. (Withdrawn) The method of claim 50 further comprising the step of implanting the ions of the second conductive type at an angle to the first surface of between 80 degrees and 90 degrees.

54. (Withdrawn) A method of manufacturing a solid picture element having a semiconductor substrate of a first conductive type with a first surface, a transistor located within the semiconductor substrate for amplifying charges, a charge accumulation region of a second conductive type located within the semiconductor substrate, the charge accumulation region having a margin located a first distance from the transistor, a depletion prevention region of the first conductive type located between the charge accumulation region and the first surface of the semiconductor substrate, the depletion prevention region having a margin located a second distance from the transistor, and a transfer gate located on the first surface of the semiconductor substrate between the depletion prevention region and the transistor overlapping a portion of the depletion prevention region margin and the charge accumulation region margin, the charge accumulation region margin being closer to the transistor than the

depletion prevention margin, the transfer gate controlling transfer of charges from the charge accumulation region to the transistor, the substrate and the depletion prevention region having different impurity concentrations, the method comprising the steps:

forming a mask layer on the semiconductor substrate, the mask layer having a mask margin located a third distance from the transistor;

implanting ions of the first conductive type into the semiconductor substrate using the mask layer as a mask and forming the charge accumulation region such that the charge accumulation region is within the semiconductor substrate and does not contact the first surface of the semiconductor transistor;

removing the mask layer;

forming the transfer gate on top of the semiconductor substrate and locating an end margin of the transfer gate such that the end margin is located a forth distance from the transistor and the fourth distance is greater than the third distance of the mask margin from the transistor; and

implanting ions of the second conductive type into the semiconductor substrate using the transfer gate as a mask and forming the depletion prevention region such that it is between the charge accumulation region and the first surface of the semiconductor substrate, and the first distance of the charge accumulation region margin to the transistor is less than the second distance of the depletion prevention region margin to the transistor.

55. (Withdrawn) The method of claim 54 wherein the third distance and the fourth distance are selected such that the first distance is not less than the second distance by more than 0.2 μm.